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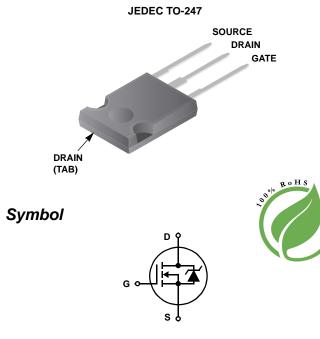
HUFA75852G3_F085

Data Sheet

December 2011

75A, 150V, 0.016 Ohm, N-Channel, UltraFET® Power MOSFET







Features

- Ultra Low On-Resistance
 r_{DS(ON)} = 0.016Ω, V_{GS} = 10V
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Qualified to AEC Q101
- RoHS Compliant

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUFA75852G3_F085	TO-247	75852G

Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

	HUFA75852G3_F085	UNITS
Drain to Source Voltage (Note 1)	150	V
Drain to Gate Voltage (R _{GS} = 20kΩ) (Note 1)	150	V
Gate to Source Voltage	±20	V
$ \begin{array}{l} \text{Drain Current} \\ \text{Continuous } (T_C = 25^{o}\text{C}, \text{V}_{GS} = 10\text{V}) \text{ (Figure 2)} \\ \text{Continuous } (T_C = 100^{o}\text{C}, \text{V}_{GS} = 10\text{V}) \text{ (Figure 2)} \\ \text{Pulsed Drain Current} \\ \end{array} $	75 75 Figure 4	A A
Pulsed Avalanche RatingUIS	Figures 6, 14, 15	
Power Dissipation PD Derate Above 25 ^o C	500 3.33	W W/ ^o C
Operating and Storage Temperature	-55 to 175	°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10sT _L Package Body for 10s, See Techbrief TB334T _{pkg}	300 260	00 Oo

NOTE:

1. $T_J = 25^{\circ}C$ to $150^{\circ}C$.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.

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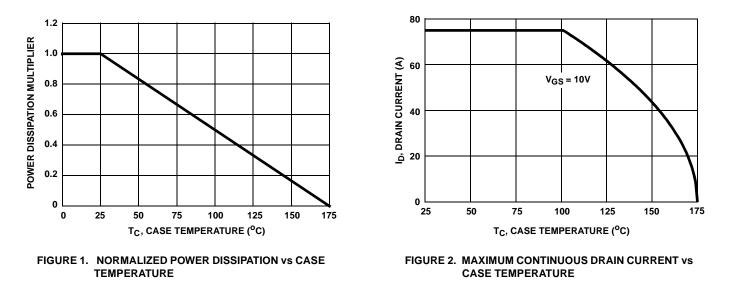
PARAMETER	SYMBOL	TEST	CONDITIONS	MIN	ТҮР	MAX	UNITS
OFF STATE SPECIFICATIONS						1	
Drain to Source Breakdown Voltage	BV _{DSS}	$I_{D} = 250 \mu A$, $V_{GS} = 0V$ (Figure 11)		150	-	-	V
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 140V, V _{GS} = 0	V	-	-	1	μA
		V _{DS} = 135V, V _{GS} = 0	0V, T _C = 150 ^o C	-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	$V_{GS} = \pm 20V$		-	-	±100	nA
ON STATE SPECIFICATIONS	ll.					I	1
Gate to Source Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 250$	μA (Figure 10)	2	-	4	V
Drain to Source On Resistance	rDS(ON)	I _D = 75A, V _{GS} = 10V (Figure 9)		-	0.013	0.016	Ω
THERMAL SPECIFICATIONS						1	1
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-247		-	-	0.30	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}			-	-	30	°C/W
SWITCHING SPECIFICATIONS (VGS	= 10V)						I
Turn-On Time	ton	V _{DD} = 75V, I _D = 75A	-	-	260	ns	
Turn-On Delay Time	t _{d(ON)}	- V _{GS} = 10V, R _{GS} = 2.0Ω	-	22	-	ns	
Rise Time	t _r	(Figures 18, 19)	-	151	-	ns	
Turn-Off Delay Time	t _{d(OFF)}			-	82	-	ns
Fall Time	t _f			-	107	-	ns
Turn-Off Time	tOFF			-	-	285	ns
GATE CHARGE SPECIFICATIONS						1	1
Total Gate Charge	Q _{g(TOT)}	$V_{GS} = 0V$ to 20V	$V_{DD} = 75V,$ $I_D = 75A,$ $I_{g(REF)} = 1.0mA$ (Figures 13, 16, 17)	-	400	480	nC
Gate Charge at 10V	Q _{g(10)}	$V_{GS} = 0V$ to 10V		-	215	260	nC
Threshold Gate Charge	Q _{g(TH)}	$V_{GS} = 0V$ to 2V		-	15	17.5	nC
Gate to Source Gate Charge	Q _{gs}			-	25	-	nC
Gate to Drain "Miller" Charge	Q _{gd}			-	66	-	nC
CAPACITANCE SPECIFICATIONS	1	1	1	I	<u>.</u>	I	L
Input Capacitance	C _{ISS}	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz (Figure 12)		-	7690	-	pF
Output Capacitance	C _{OSS}			-	1650	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	535	-	pF

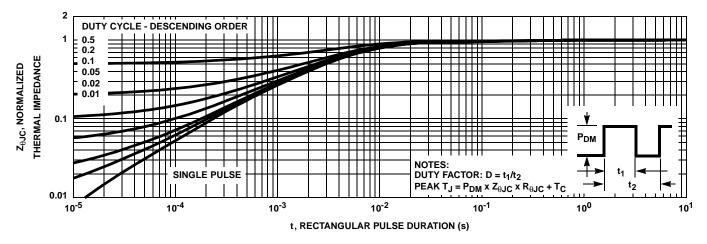
Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	ТҮР	MAX	UNITS
Source to Drain Diode Voltage	V _{SD}	I _{SD} = 75A	-	-	1.25	V
		I _{SD} = 35A	-	-	1.00	V
Reverse Recovery Time	t _{rr}	I _{SD} = 75A, dI _{SD} /dt = 100A/μs	-	-	260	ns
Reverse Recovered Charge	Q _{RR}	I _{SD} = 75A, dI _{SD} /dt = 100A/μs	-	-	1830	nC

Typical Performance Curves







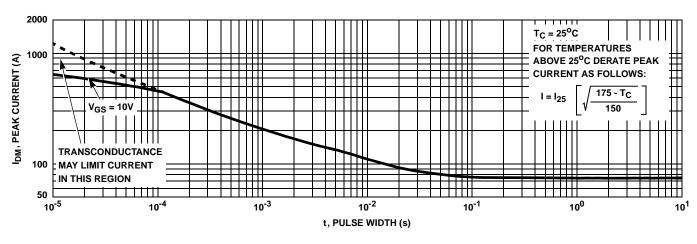


FIGURE 4. PEAK CURRENT CAPABILIT Y

Typical Performance Curves (Continued)

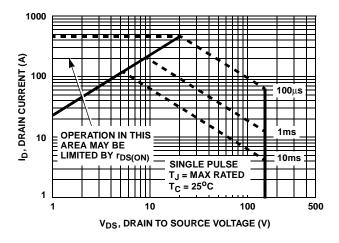


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

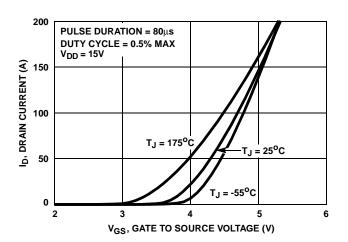
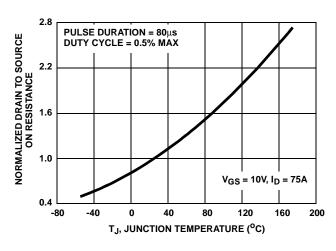
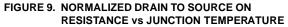
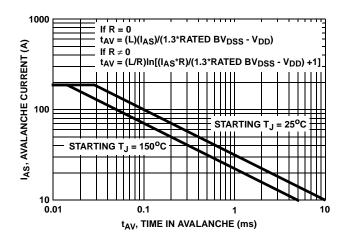


FIGURE 7. TRANSFER CHARACTERISTICS







NOTE: Refer to Fairchild Application Notes AN9321 and AN9322. FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

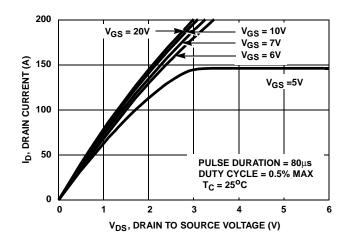
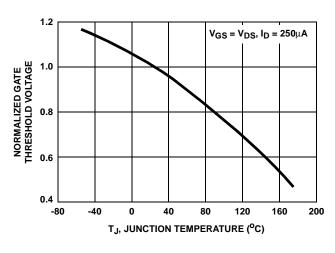
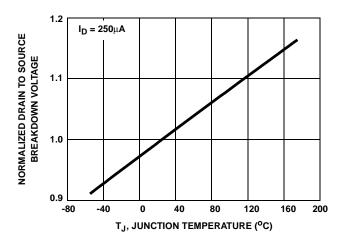


FIGURE 8. SATURATION CHARACTERISTICS





Typical Performance Curves (Continued)





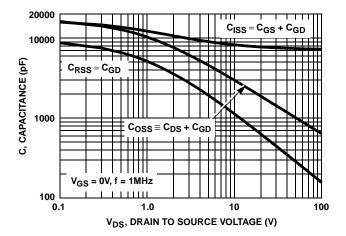
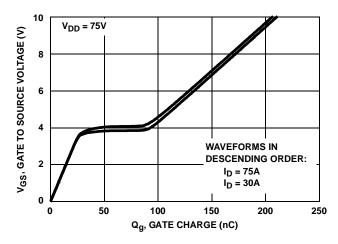


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260. FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

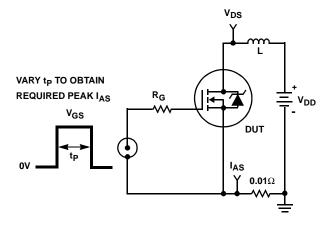


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

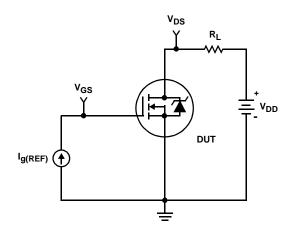


FIGURE 16. GATE CHARGE TEST CIRCUIT

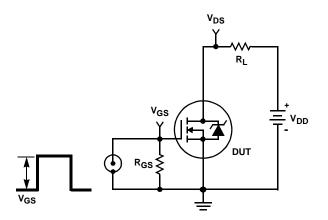


FIGURE 18. SWITCHING TIME TEST CIRCUIT

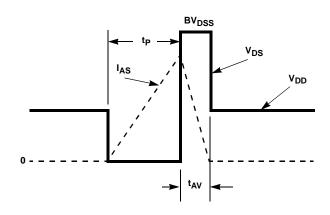


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

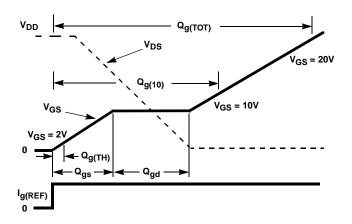


FIGURE 17. GATE CHARGE WAVEFORMS

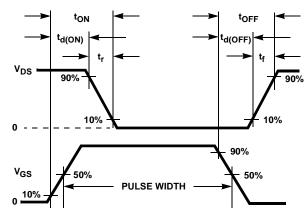


FIGURE 19. SWITCHING TIME WAVEFORM



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